UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,738	02/04/2004	Ken A. Nishimura	10030616-1	4822

57299 7590 05/02/2007

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
MOON, SEOKYUN	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
05/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/771,738	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-24* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) filed on February 04, 2004 has been acknowledged and considered by the Examiner. A copy of the form PTO-1449 is included in this correspondence.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-4, 7, 10, 13-19,** and **21** are rejected under 35 U.S.C. 102(b) as being anticipated by Kitajima et al. (US 6,064,358, herein after "Kitajima").

As to **claim 1**, Kitajima teaches a drive circuit for driving a display device [col. 1 lines 10-13] comprising electro-optical material ("*liquid crystal 57*") [fig. 11] disposed between a common electrode ("*common electrode 63*") and an array of pixel electrodes ("*display electrodes 54*") [col. 15 lines 43-46], the drive circuit comprising:

pixel drive circuits ("*thin film transistors 103*") [fig. 11] connected to respective ones of the pixel electrodes and operable to generate respective pixel drive signals ("V_D") [fig. 26(d)] alternating between a first high voltage ("V_{DH}") and a first low voltage ("V_{DL}") differing in voltage by less than or equal to a process-limited maximum ("V_{DH}"); and

a common drive circuit ("*206*") [fig. 1] connected to the common electrode and operable to generate a common drive signal ("V_C") [fig. 26(d)] alternating between a second high voltage

("*VCH*") and a second low voltage ("*VCL*") differing in voltage by more than the process-limited maximum, the common drive signal being asymmetrically bipolar with respect to the first low voltage.

As to **claim 2**, Kitajima teaches that the first low voltage ("*VDL*") and the second low voltage ("*VCL*") differ in voltage by less than or equal to a threshold voltage ("*VDH* - *VCL*") [col. 17 lines 62-64] at which an electro-optical response is produced by the electro-optical material ("*liquid crystal element*").

As to **claim 3**, Kitajima teaches that the first high voltage ("*VDH*") [fig. 26(d)] and the second high voltage ("*VCH*") differ in voltage by less than or equal to the threshold voltage ("*VDH* - *VCL*").

As to **claim 4**, Kitajima teaches the common drive signal ("*VC*") [fig. 26(d)] being substantially periodic between the second low voltage ("*VCL*") and the second high voltage ("*VCH*").

As to **claim 7**, Kitajima teaches the pixel drive circuits ("*thin film transistors 103*") [fig. 11] being located on a substrate ("*transparent glass substrate 56*") of the display device including the array of pixel electrodes ("*display electrodes 54*"), the pixel drive circuits underlying respective ones of the pixel electrodes.

As to **claim 10**, Kitajima teaches the common drive circuit ("*206*") [figs. 1 and 3] being located external to the substrate.

As to **claim 14**, Kitajima teaches at least one of the pixel drive circuits and the common drive circuit being further operable to vary the phase relationship (whether the two signals are in the same polarity phase or different polarity phase with respect to a reference level) between the respective pixel drive signals ("*VD*") and the common drive signal ("*VC*") [fig. 26(d)].

As to **claim 15**, Kitajima teaches each of the pixel drive circuits including a transistor of a size less than or equal to 180 nm [col. 9 lines 45-48].

As to **claims 13** and **16**, Kitajima inherently teaches the process-limited maximum being less than or equal to 1.8 volts which is a breakdown voltage of the pixel drive circuits since the 180 nm transistors included in the pixel drive circuits have a breakdown voltage of 1.8 volts and thus it is required for the device of Kitajima to set the process-limited maximum of the pixel drive signals being less than or equal to 1.8 volts in order to prevent breakdown of the drive circuits.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claim 1.

As to **claim 18**, Kitajima teaches the method further comprising:

determining a threshold voltage ("V_{DH} - V_{CL}") [col. 17 lines 62-64] at which an electro-optical response is produced by the electro-optical material; and

setting the first low voltage ("V_{DL}") [fig. 26(d)] and the second low voltage ("V_{CL}") to differ in voltage by less than or equal to the threshold voltage and the first high voltage ("V_{DH}") and the second high voltage ("V_{CH}") to differ in voltage by less than or equal to the threshold voltage.

As to **claim 19**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 21**, all of the claim limitations have already been discussed with respect to the rejection of claims 7 and 10.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to

a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 5** and **9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitajima in view of the Applicants' Admitted Prior Art (herein after "AAPA").

As to **claim 5**, Kitajima [fig. 26(d)] teaches that the pixel drive signal ("V_D") outputted from the pixel drive circuit which is comprised of 180 nm transistors [col. 9 lines 45-48] alternates between the first low voltage ("V_{DL}") and the first high voltage ("V_{DH}").

Kitajima does not expressly disclose the values of the first low voltage and the first high voltage.

However, AAPA teaches that 180 nm transistor has a breakdown voltage of 1.8 V [pg. 3 lines 9-10].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the pixel drive circuit of Kitajima to output a pixel drive signal alternating between 0 volts and 1.8 volts, as taught by AAPA, in order to fully utilize the acceptable driving voltage range of the pixel drive circuit, and thus to minimize the contrast degradation.

As to **claim 9**, Kitajima teaches the common drive circuit including a transistor.

Kitajima does not expressly disclose the size of the transistor.

However, AAPA teaches an idea of using 350 nm CMOS transistor to build a drive circuit of a display device [pg 3 lines 7-9].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the common drive circuit of Kitajima to use 350 nm CMOS transistors as its components, as taught by AAPA, in order to provide a more power efficient common drive circuit [pg 3 lines 4-6].

6. **Claims 8**, **11**, **20**, and **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitajima.

As to **claim 8**, Kitajima teaches the common drive circuit being located external to the substrate [figs. 1 and 3].

Kitajima does not teach the common drive circuit being located on the substrate.

However, since the Applicants have failed to disclose that implementing the common drive circuit on the substrate instead of implementing the circuit external to the substrate provides an advantage, is used for a particular purpose, or solves a state problem, it is an obvious matter of design choice to include the common drive circuit on the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the common drive circuit either on the substrate or external to the substrate since any one of the implementation would perform equally well at providing pixel drive signals and the common drive signals to display elements of a display.

As to **claim 11**, Kitajima teaches a timing circuit ("*timing signal generating circuit 204B*") [fig. 1] connected to the common drive circuit ("*206*") to control the timing of the common drive signal.

Kitajima does not expressly disclose the timing circuit being included on the substrate.

However, Examiner takes official notice that it is well known in the art to implement a timing circuit, i.e. timing controller, of a display device on a substrate which includes pixel drive circuits and pixel electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the display device of Kitajima to include the timing circuit of the device on the substrate on which the pixel drive circuits and the pixel electrodes are formed, in order to reduce the number of substrates required to implement the drive circuits of the display.

As to **claim 20**, all of the claim limitations have already been discussed with respect to the rejection of claims 7 and 8.

As to **claim 22**, all of the claim limitations have already been discussed with respect to the rejection of claim 11.

7. **Claims 12**, **23**, and **24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitajima in view of Kawaguchi et al. (US 6,677,925, herein after "Kawaguchi").

As to **claim 12**, Kitajima teaches the timing circuit ("*timing signal generating circuit 204B*") [fig. 1] alternates between the first low voltage ("V_{DL}") [fig. 26(d)] and the first high voltage ("V_{DH}") and the common drive circuit outputting the second low voltage ("V_{CL}") and the second high voltage ("V_{CH}").

Kitajima does not teach the common drive circuit converting the first low voltage to the second low voltage and the first high voltage to the second high voltage.

However, Kawaguchi teaches a display device [fig. 1] adopting a method of using pixel drive signals to generate a common drive signal [col. 23 lines 9-26].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the common drive circuit of Kitajima to use the pixel drive signals to generate the common drive signal by converting the first low voltage and the first high voltage of the pixel drive signals to the second low voltage and the second high voltage of the common drive signal, as taught by Kawaguchi, in order to simplify the structure of the voltage generating circuitry of the common drive circuit.

As to **claim 23**, all of the claim limitations have already been discussed with respect to the rejection of claim 12.

As to **claim 24**, all of the claim limitations have already been discussed with respect to the rejection of claim 14.

Allowable Subject Matter

8. **Claim 6** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (572) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

04/27/2007

- s.m.

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER